

BUK9006-55A

TrenchMOS™ logic level FET

Rev. 01 — 1 August 2003

Preliminary data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor available as a bare die using Philips General Purpose Automotive (GPA) TrenchMOS™ technology.

Product availability:

BUK9006-55A distributed as individual die on reel.

1.2 Features

- 25 A testing of individual die
- Inductive energy testing of individual die
- Life-tested to Q101 at 175 °C
- Automatic visual inspection.

1.3 Applications

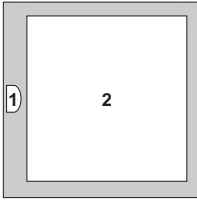
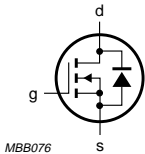
- Automotive systems
- Motors, lamps and solenoids
- 12 V and 24 V loads
- General purpose power switching.

1.4 Quick reference data

- $E_{DS(AL)S} \leq 1.1 \text{ J}$
- $V_{(BR)DSS} \leq 55 \text{ V}$
- Die size = $4.30 \times 4.30 \text{ mm}$ (typ)
- $R_{DSon(die)} = 5 \text{ m}\Omega$ (typ)
- $V_{GS(th)} = 1.5 \text{ V}$ (typ)
- Die thickness = $240 \mu\text{m}$ (typ).

2. Pinning information

Table 1: Pinning - Bare die simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate	 03nn81	 MBB076
2	source		
-	drain; connected to underside of die		



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3. Limiting values

Table 2: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

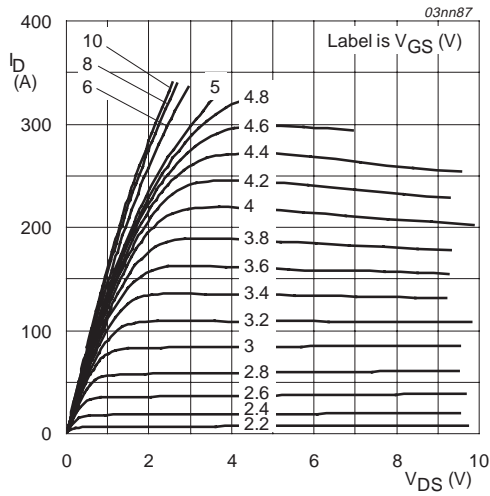
Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage (DC)		-	55	V	
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20 \text{ k}\Omega$	-	55	V	
V_{GS}	gate-source voltage (DC)		-	± 15	V	
I_D	drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}; V_{GS} = 5 \text{ V}$	[1]	-	125	A
		$T_{mb} = 100 \text{ }^\circ\text{C}; V_{GS} = 5 \text{ V}$	[1]	-	88	A
I_{DM}	peak drain current	$T_{mb} = 25 \text{ }^\circ\text{C}; \text{pulsed}; t_p \leq 10 \text{ }\mu\text{s}$	-	503	A	
T_{stg}	storage temperature		-55	+175	$^\circ\text{C}$	
T_j	junction temperature		-55	+175	$^\circ\text{C}$	
Source-drain diode						
I_{DR}	reverse drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$	[1]	-	125	A
I_{DRM}	peak reverse drain current	$T_{mb} = 25 \text{ }^\circ\text{C}; \text{pulsed}; t_p \leq 10 \text{ }\mu\text{s}$	-	503	A	
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 25 \text{ A}; V_{DS} \leq 55 \text{ V}; V_{GS} = 5 \text{ V}; R_{GS} = 50 \text{ }\Omega;$ starting $T_j = 25 \text{ }^\circ\text{C}$	-	1.1	J	

[1] Calculated with $R_{th(j-mb)} = 0.59 \text{ K/W}$.

4. Characteristics

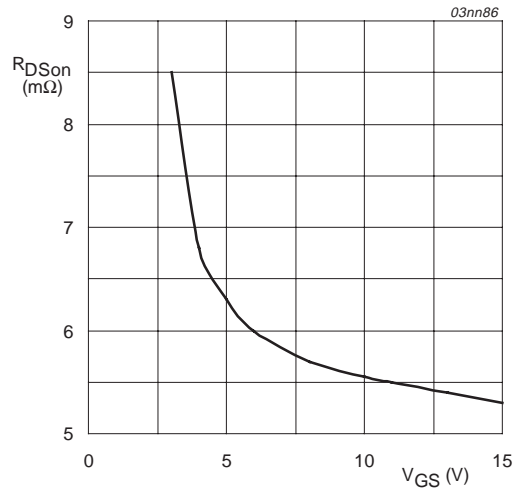
Table 3: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	55	-	-	V
		$T_j = -55\text{ °C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS};$ Figure 5				
		$T_j = 25\text{ °C}$	1	1.5	2	V
		$T_j = 175\text{ °C}$	0.5	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.3	V
I_{DSS}	drain-source leakage current	$V_{DS} = 55\text{ V}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.05	10	μA
		$T_j = 175\text{ °C}$	-	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 15\text{ V}; V_{DS} = 0\text{ V}$	-	2	100	nA
$R_{DS(on)(die)}$	die drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 25\text{ A};$ Figure 4				
		$T_j = 25\text{ °C}$	-	5	6	m Ω
		$T_j = 175\text{ °C}$	-	-	12	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$V_{GS} = 5\text{ V}; V_{DS} = 44\text{ V};$	-	92	-	nC
Q_{gs}	gate-source charge	$I_D = 25\text{ A};$ Figure 10	-	11	-	nC
Q_{gd}	gate-drain (Miller) charge		-	43	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V};$	-	4550	6020	pF
C_{oss}	output capacitance	$f = 1\text{ MHz};$ Figure 8	-	760	900	pF
C_{rss}	reverse transfer capacitance		-	500	690	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 1.2\text{ }\Omega;$	-	40	-	nS
t_r	rise time	$V_{GS} = 5\text{ V}; R_G = 10\text{ }\Omega$	-	175	-	nS
$t_{d(off)}$	turn-off delay time		-	280	-	nS
t_f	fall time		-	167	-	nS
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V};$ Figure 11	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}$	-	70	-	ns
Q_r	recovered charge	$V_{GS} = -10\text{ V}; V_{DS} = 30\text{ V}$	-	160	-	nC



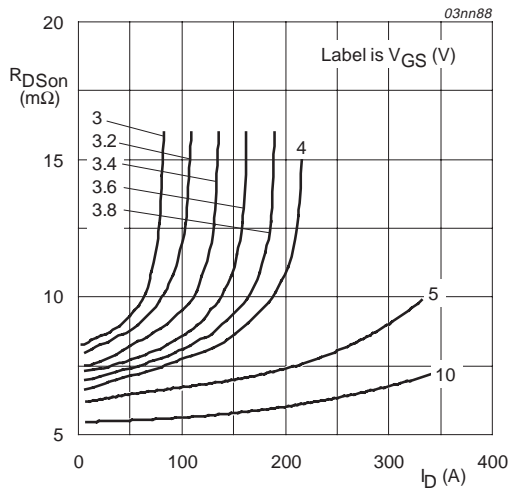
$T_j = 25\text{ }^\circ\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 1. Output characteristics: drain current as a function of drain-source voltage; typical values.



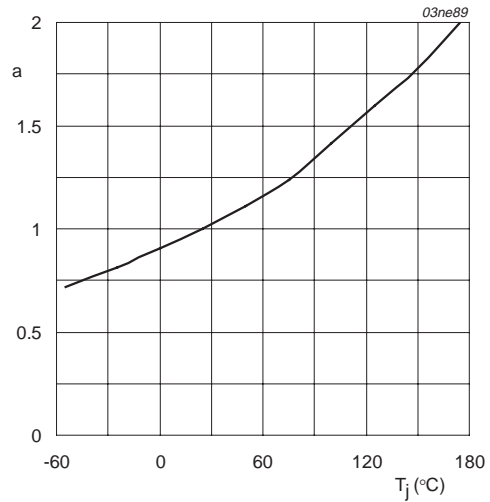
$T_j = 25\text{ }^\circ\text{C}$; $I_D = 25\text{ A}$

Fig 2. Drain-source on-state resistance as a function of gate-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$; $t_p = 300\text{ }\mu\text{s}$

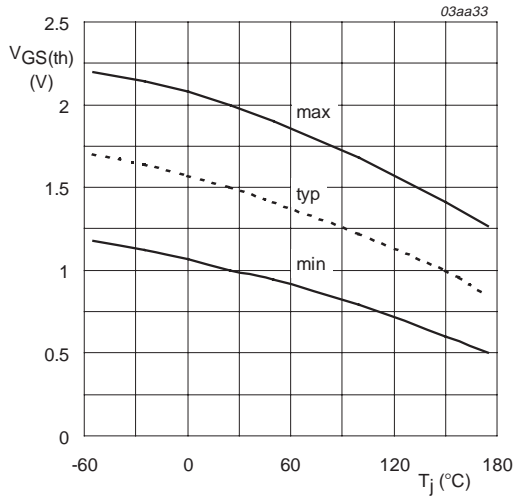
Fig 3. Drain-source on-state resistance as a function of drain current; typical values.



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

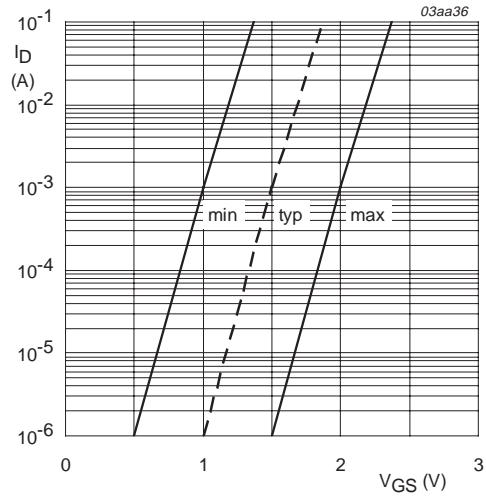
Fig 4. Normalized drain-source on-state resistance factor as a function of junction temperature.

Remark: Figures 1, 2, and 3 measured on die assembled in SOT78 with 3 x 350 μm source bond wires.



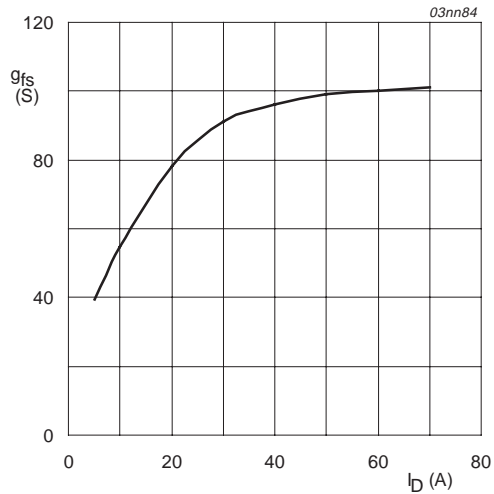
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 5. Gate-source threshold voltage as a function of junction temperature.



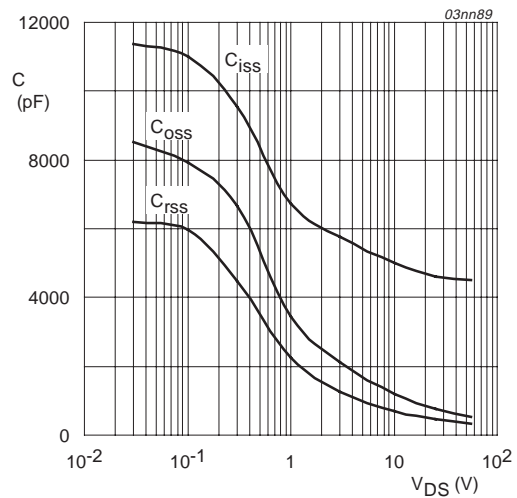
$T_j = 25 \text{ °C}; V_{DS} = V_{GS}$

Fig 6. Sub-threshold drain current as a function of gate-source voltage.



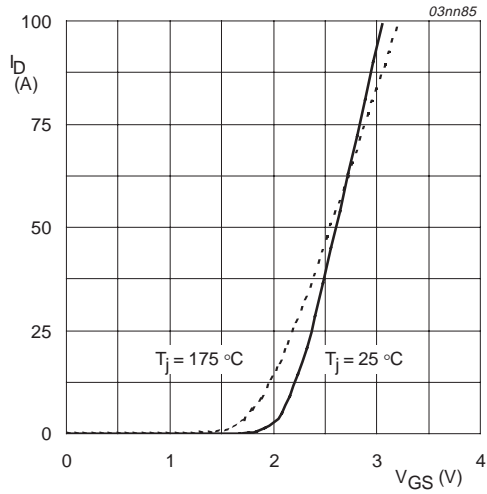
$T_j = 25 \text{ °C}; V_{DS} = 25 \text{ V}$

Fig 7. Forward transconductance as a function of drain current; typical values.



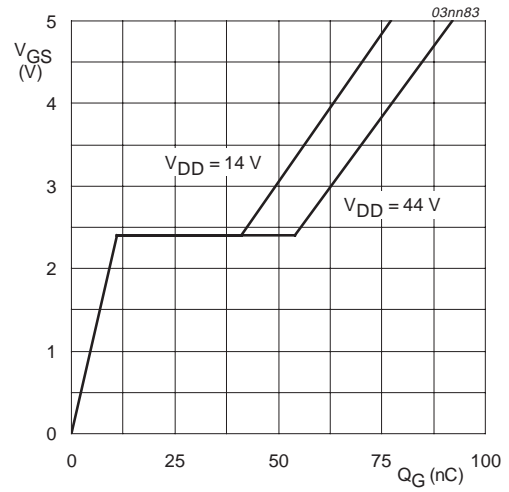
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 8. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



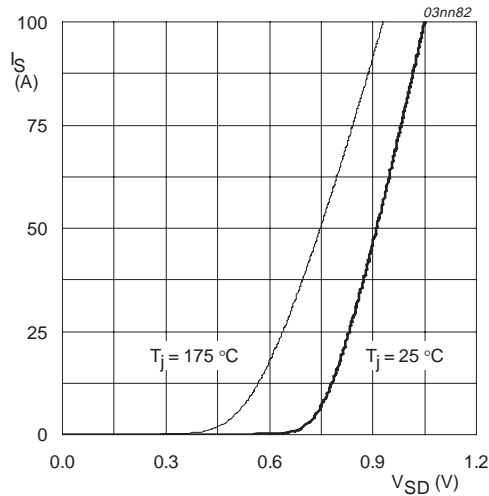
$V_{DS} = 25 \text{ V}$

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



$T_j = 25 \text{ °C}; I_D = 25 \text{ A}$

Fig 10. Gate-source voltage as a function of gate charge; typical values.



$V_{GS} = 0 \text{ V}$

Fig 11. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

Remark: Figures 9, 10, and 11 measured on die assembled in SOT78 with 3 x 350 μm source bond wires.

5. Bare die outline

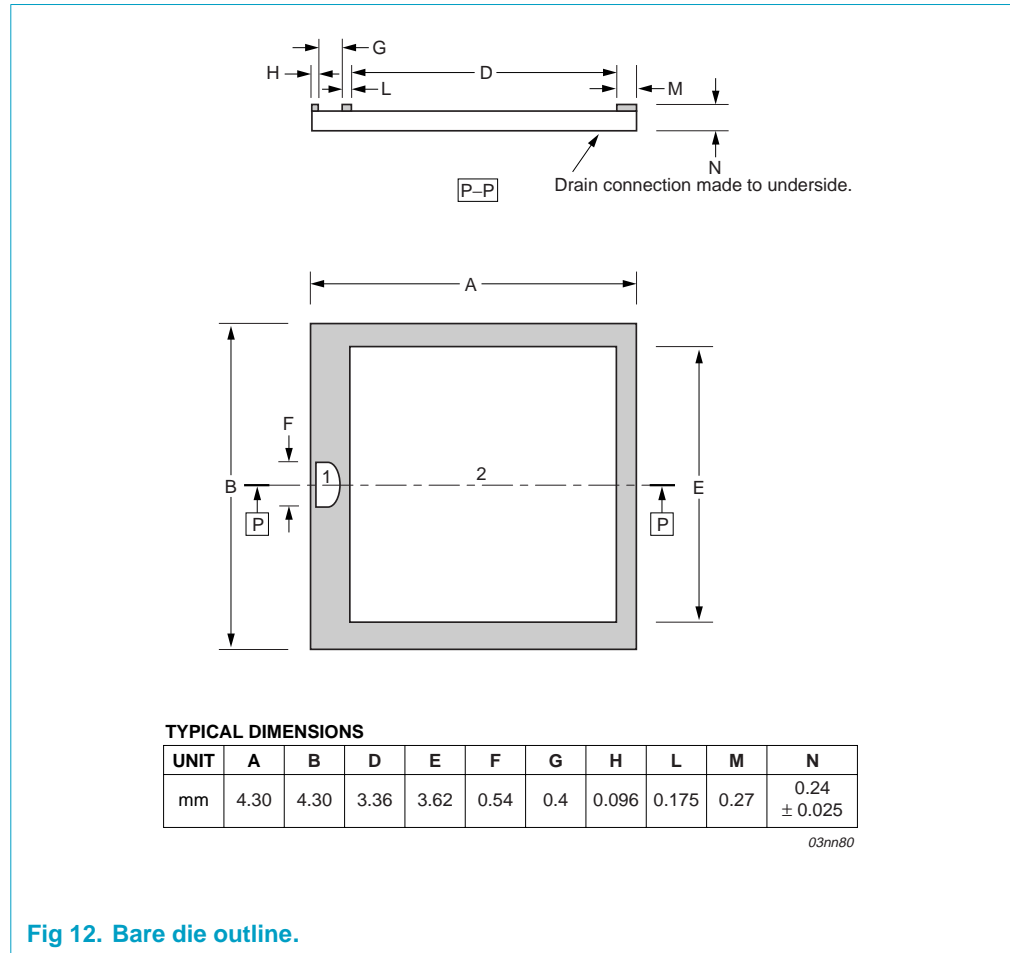


Fig 12. Bare die outline.

Table 4: Bare die information

Parameter	Description
Top-side metallization (gate and source bond pads)	5 μm Al + 1 % Si (sputtered)
Back-side metallization (drain contact)	0.1 μm Ti / 0.3 μm Ni / 0.1 μm Ag (evaporated)
Passivation layer	1 μm Si ₃ N ₄

6. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
01	20030801	-	Preliminary data (9397 750 11571)

7. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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